Design of n-Channel MOSFET Transistor for Switching of Perpendicular Anisotropy CoFeB Magnetic Tunnel Junction

Written I. Yulaev (ivan_yulaev@yahoo.com)

2011-03-17

ECE135B Final Project

Winter 2011, taught by Professor Paul Yu

0 Contents

0.1 Table of Figures

0.2 Table of Tables

0.3 Table of Equations

1 Abstract

We design a transistor, compatible with the Intel 32nm CMOS process, capable of driving a current for switching the magnetization of a CoFeB/MgO perpendicular anisotropy spin valve. We demonstrate that sufficient current can be obtained by using a transistor with W-L aspect ratio equal to 1, given sufficient but reasonable choices for V_G, V_{DD}, and V_T. After developing a simulation model based on the gradual channel approximation and taking into account practical non-idealities of sub-micron devices, we characterize the transistor's performance characteristics. Our results show that implementation of MTJ-based STT-MRAM cells in a modern 32nm CMOS process does not necessitate the use of transistors with excessively wide gates, and that CMOS technology is not a limiting factor in the scaling of CoFeB/MgO spin valves to the 32nm node.

2 Foreword

This paper represents my [Ivan Yulaev's] submission for the ECE135B Winter 2011 Final Project. For the benefit of the grader, this section will discuss the guidelines we intend to meet, and which sections of this report pertain to which guideline requirements. We attempt to meet the following guidelines in this paper:

A. We specify the objectives of the design; **this is done in section 3.2**.
B. We specify the parameters for the device, and the assumptions made for the device. **This is done in section 3.2.1 and 3.2.2.**
C. We draw a preliminary physical layout. **This is captured in section 3.3**
D. We discuss the design process, and the model that we will use to simulate the performance of our transistor and find an optimal set of physical parameters. **This is done in section 4.1 - 4.4.**
E. We present a performance characterization of the device, including device output characteristics. **This is presented in section 4.5.**
F. We also present a final physical layout of the device; **this is done in section 4.5.1.**
G. We discuss our results, comment on their accuracy, and give guidance as to the significance of our findings. **This is done in section 5.**

Any questions should be directed to Ivan Yulaev, reachable at ivan_yulaev@yahoo.com.

3 Introduction of Goal and Design Assumptions

In this section, we introduce the goal of the transistor design. We will first discuss the intended application for the particular transistor that we are designing and modeling, and then describe the model used and the assumptions made.

3.1 Introduction to Magnetic Tunnel Junctions

Magnetic Tunnel Junctions present a promising structure for implementing non-volatile, high-density memory in CMOS logic integrated circuits (1). In particular, the perpendicular anisotropy CoFeB/MgO/CoFeB structure has characteristics making it suitable for such an application, such as low switching current and good thermal stability. In a perpendicular anisotropy MTJ, a free magnetic element within the structure is aligned in one of two directions; due to the TMR effect (2), the resistance of the structure is low when the free magnetic element has magnetization that is in parallel alignment with a fixed reference element, and the resistance increases when the alignment is anti-parallel. This is illustrated schematically in Figure 1. The magnetic orientation of the free magnetic element can be used to store a single bit of information.

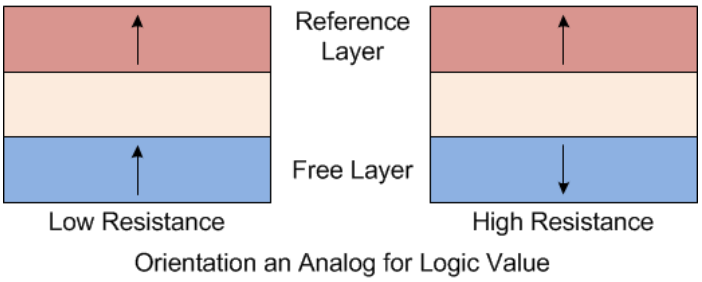

Figure 1 - Schematic Illustration of MTJ Orientations and Corresponding Logic Values

Switching of magnetization orientation can be accomplished by driving a current through the magnetic pillar (3). The current is spin polarized by the reference layer. Due to the spin torque transfer effect, this spin polarization exerts a net torque on the magnetization of the free layer. A sufficiently large current can provide a torque strong enough to induce switching of magnetization for the free layer. This operation is analogous to “writing” a logical value into our MTJ-based memory cell.

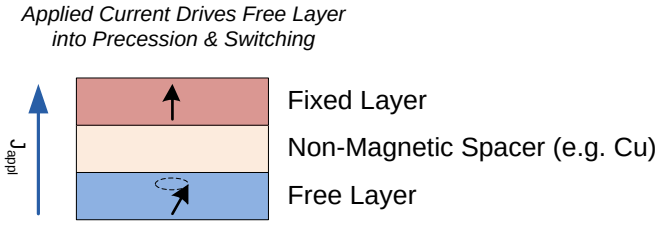

Figure 2 - Schematic Illustration of Applied Current Switching Magnetization in MTJ Element

A thorough discussion of spin torque transfer and GMR/TMR resistance change is outside of the scope of this paper; the reader is referred to the excellent paper by Ralph and Stiles that is cited in section 6.

Several obstacles present themselves when scaling MTJ-based memory elements deep into submicron length scales. One of the limitations in scaling is that switching current requirements remain fairly constant irrespective of device volume (4); switching current (I_C) remains in fairly constant proportion to the energy barrier to switching (E_B). Since E_B cannot be reduced below roughly 45kT without compromising thermal stability, to the first order, there is a floor on I_C in MTJ structures. When scaling such a structure, due to the reduced size of the nanopillar, the applied current density must increase. The challenge for the semiconductor engineer is thus to implement a small transistor (in terms of IC die area) that can provide enough current to switch the magnetization of the free magnetic element. In this paper, we present the design of an n-channel MOSFET, based on the Intel 32nm logic IC process (5), which provides sufficient drive current to switch the free magnetic element in a CoFeB/MgO spin valve, while minimizing overall transistor area.

3.2 Transistor Design Assumptions and Circuit Setup

We make some simplifying assumptions to abstract away some of the complexity associated with the behavior of MTJ-based magnetic memory devices. In our analysis, we will model the tunnel junction as a resistance with magnitude 7kΩ (1), as illustrated in Figure 3. **We will assume that the minimum required switching current will be 49µA**, although larger values of drive current will enable us to switch the MTJ-based device in shorter time scales. In this circuit setup, we design our transistor to maintain this drive current, aiming to minimize feature size. We will also attempt to characterize and optimize the performance of the device, for example by reducing standby and dynamic power consumption, improving frequency response, etc. A floor for the channel length is set by the Intel 32nm process.

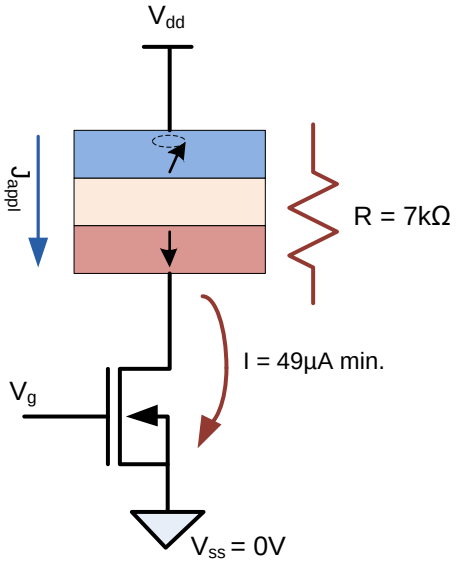

Figure 3 - Equivalent Circuit with MTJ Represented as Series Resistance

Our design process will proceed by first defining an operational range and physical parameter space for our device to operate within. We will pick a preliminary layout, somewhere near the middle of the parameter space. We will then run simulations/calculations inside of this parameter space, and determine how to best meet the design requirements set out earlier in this section.

We define the operational range of our MOSFET by selecting the absolute maximum parameters within which it can operate; these parameters are enumerated in the below table.

Table 1 - Operational Range and Parameter Space for MOSFET Design

Parameter (Units)	**Min (Units)**	**Max (Units)**
V_{DD}[1,2]	0.9V	1.4 V
V_G[3]	-0.3V	V_{DDMAX}
Gate Length L	32 (nm)	32 (nm)
Gate Width W	32 (nm)	(n/a)[4]
Channel Doping N_A (units/cm^3)[5]	2 x 10^{18}	2 x 10^{19}
V_T	0.2V	0.7V

Notes:

1. *Obtained from V_{CCMIN} distribution for Intel 32nm process; see fig. 16 in* (5)
2. *Taken from Intel Core i7 Datasheet* (6)*, Absolute Maximum V_{DD} (table 43)*
3. *We assume no voltage higher than V_{DD} may exist in our system.*
4. *There is no practical maximum for gate width; however, we will attempt to minimize this as this is a key contributor to transistor area.*
5. *Channel doping is designed particularly to control W_{dm}, to minimize drain-induced barrier lowering [Taur 183].*

For N_C, N_V, n_i we will use 3.2 x 10^{19}, 1.8 x 10^{19}, and 1.0 x 10^{10} respectively (7). For saturation velocity we will use v_s = 1.0 x 10^7 cm/s. For mobility μ_n, will assume it follows the relationship with (large) applied field E [Taur 170], and is limited to 1,400 otherwise (7).

Equation 1 -Electron Mobility for High Applied Field Conditions

$$\mu_{eff} = \min(1400, 32500 \times E_{eff}^{-1/3})$$

In our design process, we will primarily use the **gradual channel approximation** for calculation of current-voltage characteristics. We will include the non-ideal effects of

1. Channel length modulation
2. Velocity saturation
3. Variation in mobility based on applied field in silicon bulk (but not due to strain nor $N_A$concentration)
4. Parasitic source-drain resistance
5. Sub-threshold conduction

3.2.1 Simplifying Assumptions

To simplify our analysis, the following assumptions regarding device layout and structure will be made. Note that these are mostly likely not completely accurate, although they should be reasonable to use when modeling the performance of real-world devices.

1. We will assume uniform doping of the SC bulk.

2. Quantum effects on inversion layer depth will be ignored.
3. We will ignore gate depletion effects. Modern transistors use metal gates which do not have the same gate depletion effect as poly-Si gate, so this is a fairly realistic assumption.
4. We will ignore gate leakage and gate breakdown; high-k gate dielectrics used in modern processes appear to mitigate this issue.
5. We will ignore parasitic capacitances, other than the gate capacitance. This assumption is somewhat unrealistic; in modern MOSFETs a sizable proportion of capacitance comes from gate-to-contact capacitance and from fringing fields.

3.2.2 Threshold Voltage and Oxide Capacitance

In our model, threshold voltage will not be calculated separately. It will be taken as a parameter that we can freely modify within the range defined earlier. The reasoning for this is that in most modern processes, non-uniform in the Si bulk can produce arbitrary V_T for given W_{dm} [Taur 224]. Furthermore, trapped charge and choice of gate material can impact V_T significantly; Q_t and X_m consistent with dual band-edge polysilicon gates is no longer an appropriate starting point for modern VLSI circuits.

For oxide capacitance, we will assume that we are using SiO_2, at the maximum thickness for a 32nm channel length ≈ L/20 = 1.6nm. This thickness is the maximum thickness allowed to maintain controllable short channel drain-induced barrier lowering [Taur 181-184] and also to maintain a fairly low sub-threshold conduction slope [Taur 166]. Assuming $\varepsilon_{ox} = 3.9\ \varepsilon_0$, this gives us $C_{OX} = 2.2 \times 10^{-6}$ F/cm^2. We will use this figure as our nominal C_{OX} value.

3.3 Preliminary Physical Layout

Based on the assumptions made prior in this section, our preliminary physical layout will look as below, with transistor parameters noted.

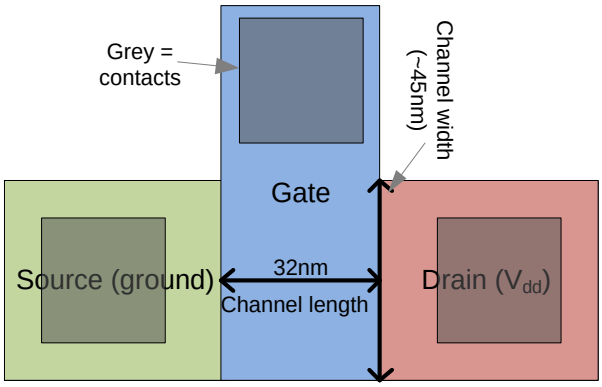

Figure 4 - Transistor Layout, Overhead View

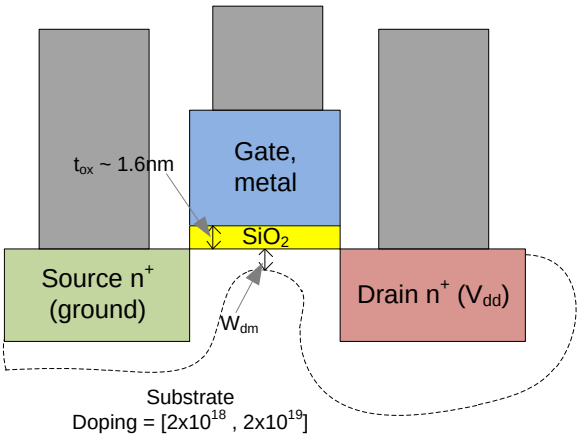

Figure 5 - Transistor Layout, Side View

4 Analysis & Simulation Results

In this section, we discuss the results of our simulation, specify which parameters we will pick for our transistor, and characterize the device performance characteristics for our final design.

4.1 Overview of Simulation Model

Our initial calculation will be of I_D across a parameter space of V_D, V_G, V_T, and other values. We use the piecewise-continuous Velocity Saturation model outlined by Taur p. 191. We model non-saturated source-drain current by the charge-sheet model, modified to take into account velocity saturation. Also, we modify L from the zero-field length of L_0 by using the below formula [Yu lect 13 slide 5].

Equation 2 - Non-saturated Drain-Source Current via Charge Sheet Model

$$I_{ds} = \frac{\mu_{eff} C_{ox} {}^{W}/_{L} \left[(V_{gs} - V_t) V_{ds} - \left(\frac{m}{2}\right) V_{ds}^2 \right]}{1 + \left(\mu_{eff} V_{ds} / 2 v_{sat} L\right)}$$

$$m = 1 + \frac{\sqrt{e_{si} q N_a / 4\psi_B}}{C_{ox}}$$

$$L = L_0 - \Delta L = L_0 - \frac{\varepsilon_{si}}{q N_A} [\sqrt{F_S^2 + 2 \frac{q N_A}{\varepsilon_{si}} (V_{ds} - V_{dsat})} - F_S]$$

We find the onset of saturation by calculating V_{dsat} and I_{dsat} using the piecewise-continuous model. This model describes the saturation behavior of electrons, while avoiding extensive mathematics [Taur 191]. We find the expressions to be as below

Equation 3 - Expression for V_{dsat} and I_{dsat} under Piecewise-Continuous Model for Electron Current Saturation

$$I_{dsat} = \frac{\mu_{eff} C_{ox} {}^{W}/_{L} \left[(V_{gs} - V_t) V_{dssat} - \left(\frac{m}{2}\right) V_{dsat}^2 \right]}{1 + \left(\mu_{eff} V_{dsat} / 2 v_{sat} L\right)}$$

$$V_{dsat} = \frac{(V_{gs} - V_t)/m}{1 + \mu_{eff} (V_{gs} - V_t) / (2 m v_{sat} L)}$$

Sub-threshold current will be calculated as for long channel MOSFETs. We will use the equation [Taur p. 165]

Equation 4 - Expression for Sub-threshold Conduction Current

$$I_{ds} = \mu_{eff} C_{ox} {}^{W}/_{L} (m-1) (\frac{kT}{q})^2 e^{\frac{q(V_{gs} - V_t)}{mkT}} (1 - e^{-\frac{qV_{ds}}{kT}})$$

4.2 Optimization Process

We optimize our design to meet the goals outlined in section . The optimization process begins by choosing parameters within the parameter space, and using our model to explore within the parameter space, with the goal of finding locations that best fit our design criteria. Using this process, we find the combination of parameters that gives a transistor capable of providing sufficient drive current, while minimizing transistor area.

4.3 N_A Selection

We select N_A based on the $L \geq 2(W_{dm} + 3t_{ox})$ rule for MOSFET design. [Taur 183]. Since our t_{ox} is 1.6nm, we find N_A that works with L = 32nm. This requires $W_{dm} \leq 11$nm; a plot of W_{dm} vs N_A (Figure 6) suggests that **the appropriate value for N_A (the bulk silicon doping concentration) is ≥1.16 x 10^{19} / cm^3.**

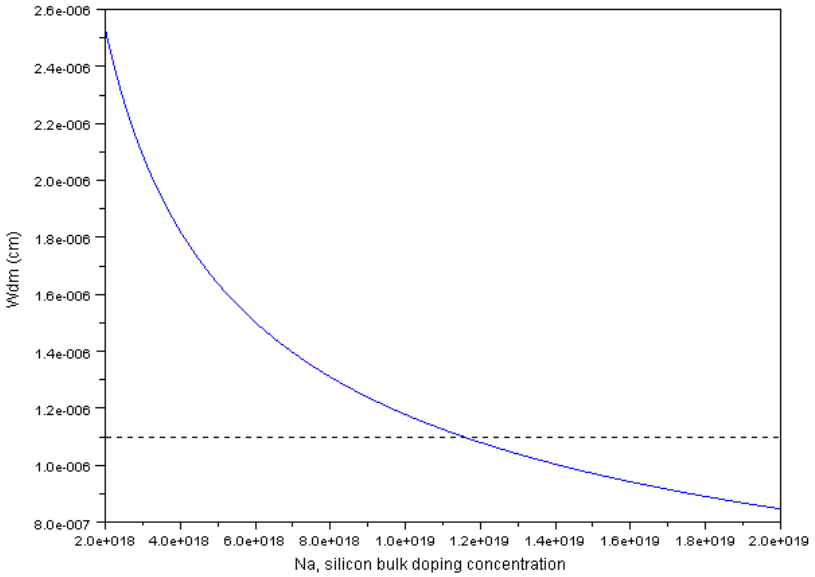

Figure 6 - Plot of W_{dm} vs N_A

This plot is based on the formulation for W_{dm} as below.

Equation 5 – Expression for Maximum Depletion width W_{dm}

$$W_{dm} = \sqrt{\frac{4\varepsilon_{si} kT ln(N_A/n_i)}{q^2 N_A}}$$

The above value of N_A ensures that the V_T reduction due to short-channel effects, i.e. via drain-induced barrier lowering, will be no worse than 0.1V [Taur 182].

4.4 Exploration of V_{DD}, V_G, V_T Parameter Space

After choosing N_A in the previous section, we explore the parameter space defined by the three voltages V_{DD}, V_G, and V_T. Plotting the classic V_{DD} / I_D curves (Figure 7) for different V_G, we find that our MOSFET is so velocity saturated, that a choice in V_{DD} hardly makes a difference, except that it also dictates the V_G that will be applied. Current saturation appears to occur at $V_{DS} \approx 0.1$V. So, we eliminate V_{DD} by itself as a parameter significant to our considerations.

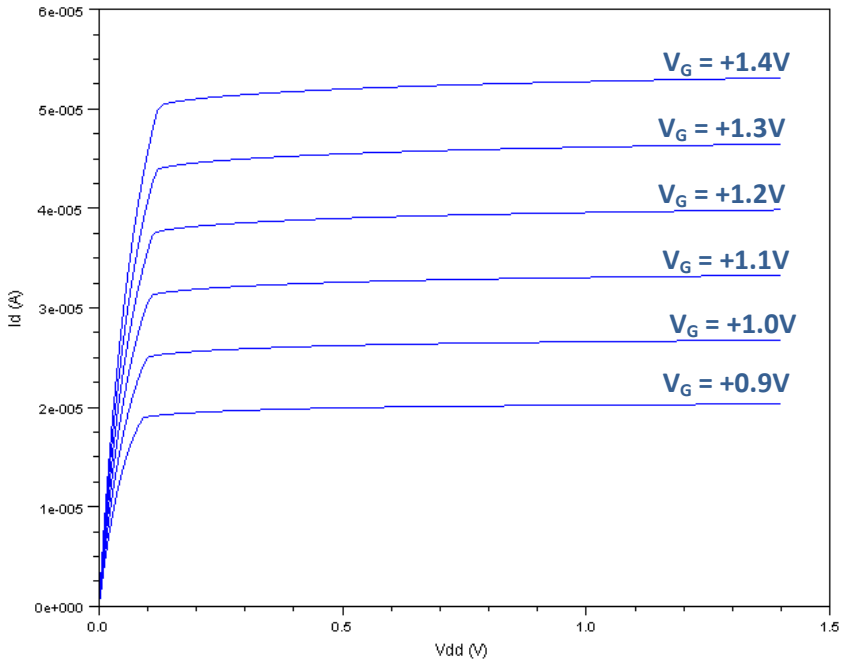

Figure 7 - Plot of I_D vs V_{DD} curves, W = 32nm, V_T = 0.4V, V_G = 0.9V to 1.4V

We next observe the effects of V_T and V_G insofar as their effect on saturation current. We can find the parameter space in the (V_G, V_T) domain where I_{DS} satisfies the criteria set forth in section 3.2, namely I_{DS} ≥ 49µA. We find that even with W/L = 1, we have a sizable parameter region where I_{DSAT} > 49µA. This can be seen in the two figures below. *The discontinuities in Figure 8 below come from the transition from sub-threshold to saturation conduction in our piece-wise model; they are non-physical phenomena.*

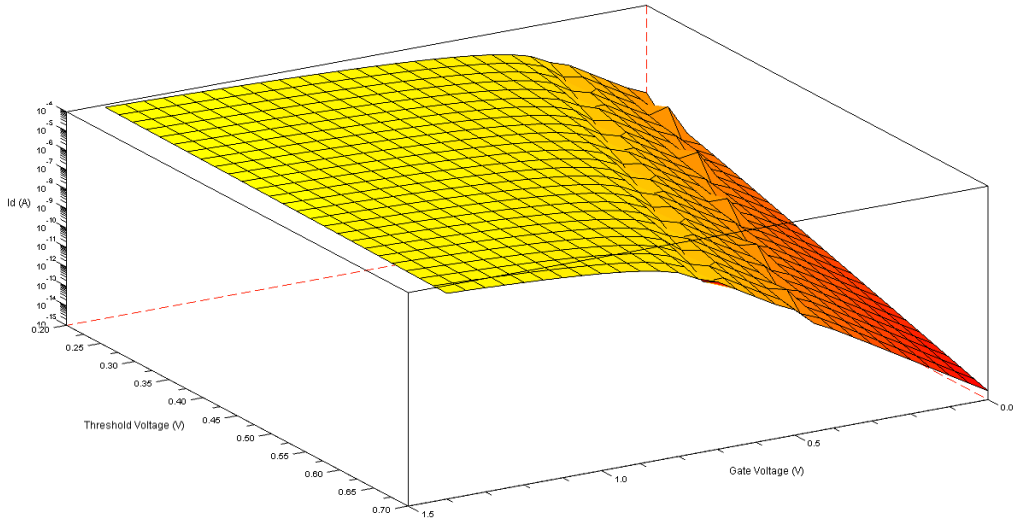

Figure 8 - Plot of I_D vs V_G/V_T, for V_D = 1.4V

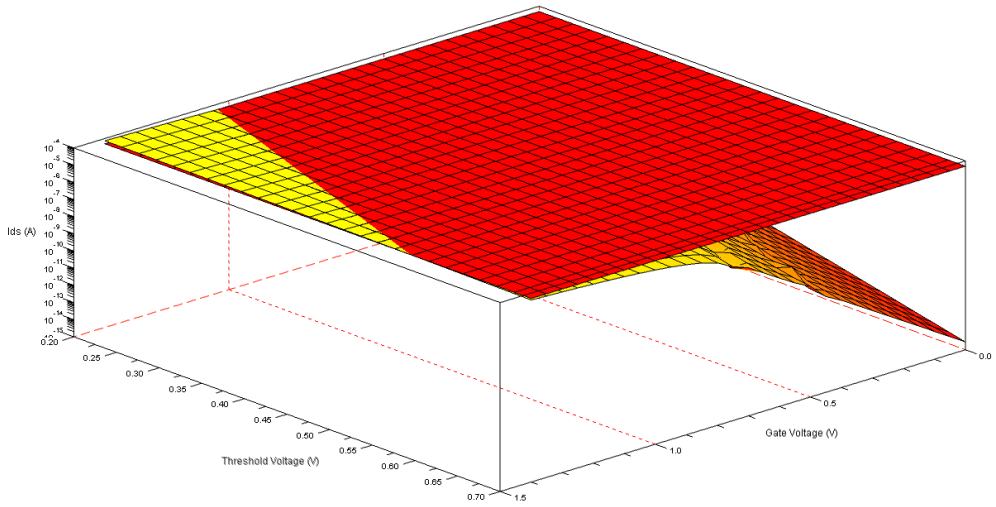

Figure 9 - Plot of I_D vs V_G/V_T, for V_D = 1.4V; Solution Space Satisfying $I_{D,min}$ = 49µA Highlighted Yellow

In Figure 9 above, we can see the region where I_D > 49µA highlighted in yellow. It is a triangle bounded by V_T = 0.55V and V_G = 1.025V; any of the (V_G, V_T) pairs in this region satisfy our constraints. **We will choose a solution roughly in the middle of this line, slightly inside the solution space, corresponding to V_G = +1.2V, V_T = +0.30V.**

4.5 Final Device Layout and Performance Characterization

Based on the device parameters chosen earlier in this section, we draw the final layout of our device, and perform a performance characterization.

4.5.1 Final Physical Layout and Device Parameters

The final physical layout for the device is captured below.

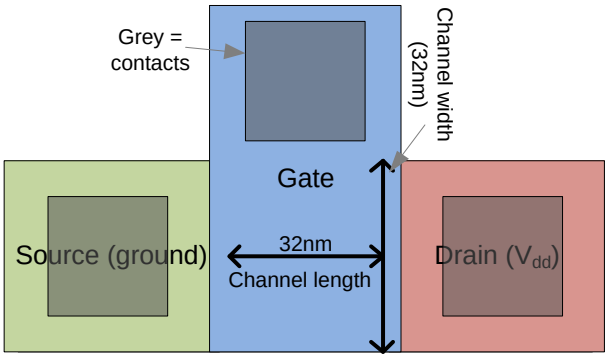

Figure 10 - Final Transistor Layout, Overhead View

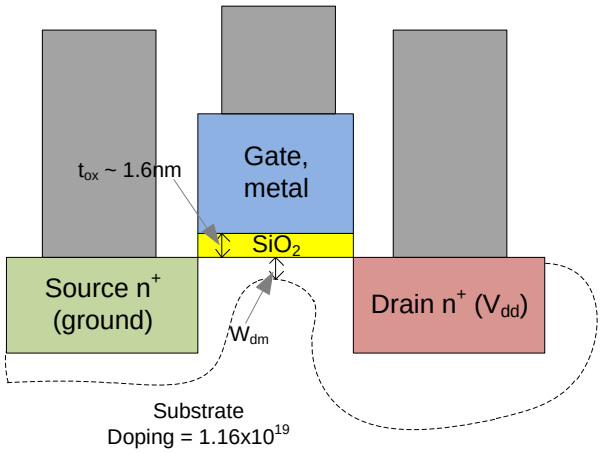

Figure 11 – Final Transistor Layout, Side View

The final device parameters are enumerated in the following table

Table 2 – Final Device Physical Parameters

Parameter (Units)	**Value (Units)**
V_{DD} [1,2]	1.2V
V_G [3]	$\leq V_{DD}$
Gate Length L	32 (nm)
Gate Width W	32 (nm)
Channel Doping N_A (units/cm^3) [5]	1.16×10^{19}
V_T	0.3V

4.5.2 Derived Parameters

In this section, we enumerate some derived parameters that are a direct result of the physical parameters captured in Figure 10, Figure 11, and Table 2.

Table 3 – Final Device Derived Parameters

Parameter (Units)	**Value (Units)**
C_{OX} (F/cm^2)	2.15×10^{-6} F/cm^2
C_{GATE} (F) [1]	2.21×10^{-17} F
I_{on}, V_G = 1.2V	53.2µA
I_{off}, V_G = 0V	140.1pA
$P_{sub\text{-}threshold}$ [2] (W), V_g = 0V	0.168nW
$P_{sub\text{-}threshold}$ (W), V_g = 0.1V	2.47nW
P_{on} (W) [3]	44µW
g_m [4] (A/V)	778nA/mV

Notes:

1. *This number ignored fringing fields and capacitance to the contacts; for the MOSFET geometry in our case this is almost certainly an optimistic assumption.*
2. *We assume that V_G is 0V for calculation of $P_{sub\text{-}threshold}$. This is almost certainly an optimistic assumption; more discussion on this is provided in Section 5.*
3. *We assume that the pull-up resistance is 7kΩ and that all parasitic resistances in the MOSFET contribute to the MOSFET power dissipation.*
4. *We use the formula $g_m = \mu_{eff} \frac{W}{L} C_{ox}(V_g - V_t)$ [lecture 12 slide 1]. Note that this assumes that the MOSFET is saturated, i.e. V_g = 1.2V.*

4.5.3 I_D vs V_D, V_G Characteristics

The I_D vs V_D characteristics are captured in Figure 12. The I_D vs V_G characteristics are captured in Figure 13.

Sub-threshold device operation (I_D vs V_G) is captured in Figure 14. Note that here, we use the n=∞ expression for V_{dsat}, as otherwise we have a discontinuity in our sub-threshold current calculation. We use the expression for V_{dsat}

Equation 6 - Expression for V_{dsat} in the n = ∞ approxiation for Velocity Saturation

$$V_{dsat} = \frac{V_{gs} - V_T}{m} + \frac{Lv_{sat}}{\mu_{eff}} - \sqrt{(\frac{V_{gs} - V_T}{m})^2 + (\frac{Lv_{sat}}{\mu_{eff}})^2}$$

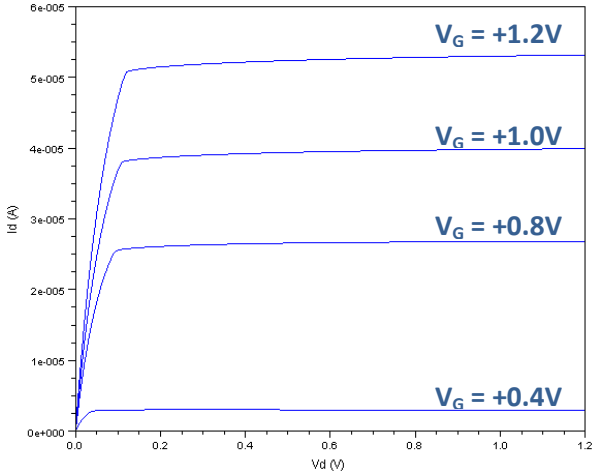

Figure 12 - I_D vs V_D Characteristics

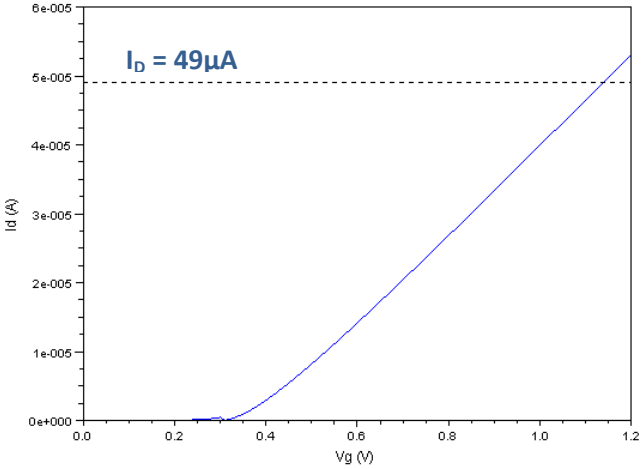

Figure 13 - I_D vs V_G Characteristics, V_{DD} = +1.2V

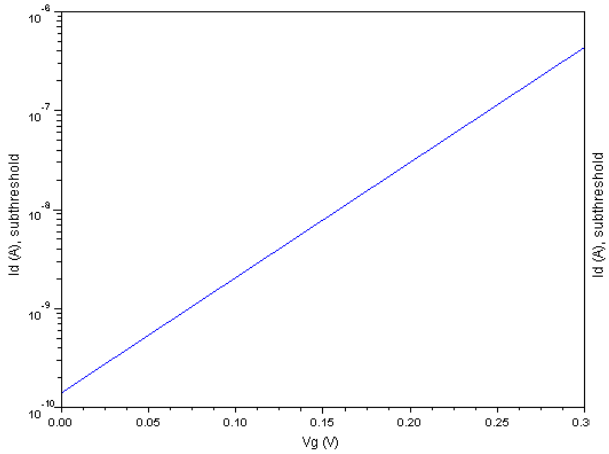

Figure 14 - I_D vs V_G Characteristics, Sub-Threshold Region of Operation (V_{DD} = +1.2V)

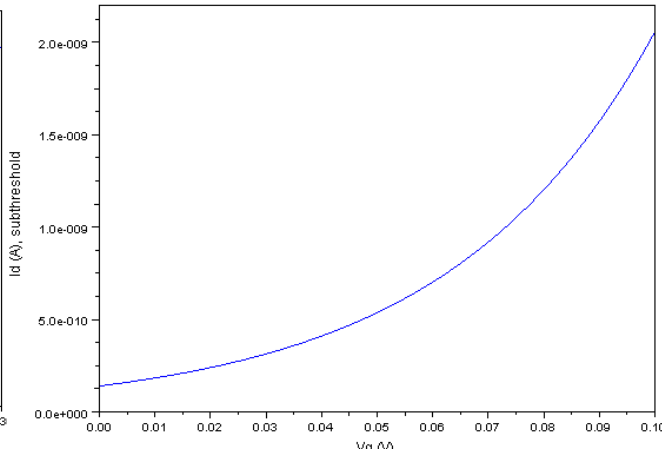

Figure 15 - I_D vs V_G Characteristics, Deep Sub-Threshold Region of Operation (V_{DD} = +1.2V)

5 Conclusion

In this paper, we have gone through the design and specification process for designing a transistor capable of driving a 49µA current through a 7kΩ load, compatible with the modern Intel 32nm process. We have demonstrated that such a transistor can be fabricated by using a gate width equal to the channel length, that is, W and L both equal to 32nm, given particular and not unreasonable choices for V_{DD}, V_G, and V_T. Furthermore, we have defined a solution space wherein V_{DD}/V_G and V_T values may be chosen to provide the required current. **The solutions space, even for a W/L=1 transistor is fairly broad and this demonstrates that scaling of STT-MRAM memory cells down to 32nm transistor sizes does not necessarily imply having to use gate widths significantly greater than the minimum defined by process capability.**

Comparing our simulation results from those published in the Intel 32nm logic paper, we find that our transistor, given V_{DD} & V_G = 1.0V and V_T = 0.3V, produces an on-current of 1.24mA. The Intel paper suggests that the on-current for their transistors, with V_{DD} = 1.0V, gives 1.62mA/µm. Thus, we are in the ballpark, considering we do not account for strain-induced mobility gain which may account for some or all of this difference. However, our off-current for the same configuration is 4.44nA/µm, while the Intel paper gives 100nA/µm; our model does not produce such off current until $V_T \leq 0.184$V. At this V_T, our on-current is 1.49mA/µm, **suggesting that our model is quite close to realistic device behavior.**

As a concluding remark, the solution space afforded a W/L=1 transistor, according to Figure 9, may seem somewhat small. Our choice of V_G and V_T provides us a saturation-limited drive current of 53.2µA, exceeding the requirement by a mere 8.5%. This result is worrisome from the production standpoint, as channel length variations in a process may result in fabrication of transistors that are unable to switch the MRAM memory element they are connected to, ultimately resulting in non-functional memory cells. In our analysis, we have ignored one critical element of modern transistor design and fabrication: the use of SiGe in the transistor body to induce strain in the channel-area silicon. Recent empirical measurements suggest that use of $Si_{0.7}Ge_{0.3}$ for the transistor body can result in a mobility improvement of up to 110% under high field conditions (8). Even if we use a more pessimistic factor of 1.6 for mobility gain due to strained Si, our solution space, as seen in Figure 16, is greatly increased. This gives us additional room to potentially decrease V_{DD}/V_G and increase V_T in order to lower our dynamic and static power consumption respectively.

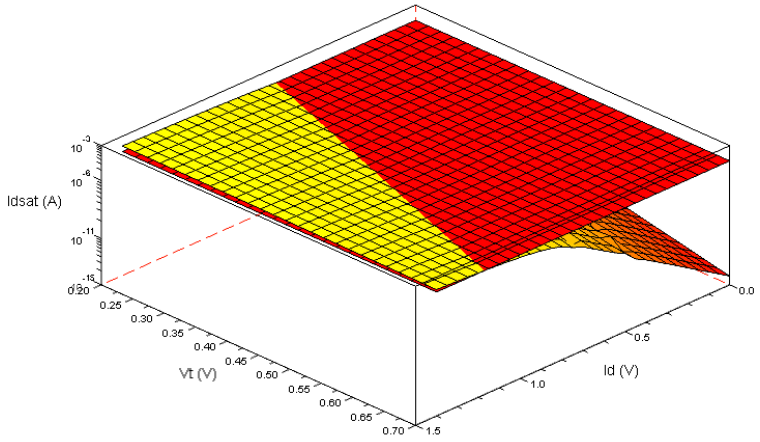

Figure 16 - Solution Space for I_{DSAT} > 49µA assuming strain-induced mobility gain of 1.6x

6 Works Cited

1. *A perpendicular-anisotropy CoFeB-MgO magnetic tunnel junction.* **S. Ikeda, K. Kiura, H. Yamamoto, K. Mizunuma, H.D, Gan, M. Endo, S. Kanai, J. Hayakawa, F. Matsukura, H. Ohno.** September 2010, Nature Materials, Vol. 9, pp. 721-724. 10.1038/NMAT2804.

2. **W.H. Butler, X.G. Zhang, T.C. Schulthess, J.M. MacLaren.** 63, s.l. : Physics Rev. B, 2001. 054416.

3. *Current-driven excitation of magnetic multilayers.* **Slonczewski, J.C.** 159, s.l. : Journal of Magnetism and Magnetic Materials, 1995. S0304-8853(96)00062-5.

4. *Macrospin models of spin transfer dynamics.* **Jiang Xiao, A. Zangwill, M. D. Stiles.** 72, s.l. : Physical Review B., 2005. 014446-1.

5. *High Performance 32nm Logic Technology Featuring 2nd Generation High-k + Metal Gate Transistors.* **Intel Corporation.** Hillsboro : s.n., 2010.

6. **Intel Corporation.** *Intel Core i7-600, i5-500, i5-400, i3-300 Mobile Processor Series Datasheet.* s.l. : Indel Corporation, 2010. 322812-001.

7. Physical Properties of Silicon (Si). *Ioffe Physical Technical Institute.* [Online] Ioffe Physical Technical Institute. [Cited: 03 07, 2011.] http://www.ioffe.ru/SVA/NSM/Semicond/Si/.

8. *Moore's Law past 32nm: Future Challenges in Device Scaling.* **Kuhn, Kelin J.** Beijing : Intel Corporation / IWCE, 2009.

9. **Yuan Taur, Tak H. Ning.** *Fundamentals of Modern VLSI Devices.* New York : Cambridge University Press, 1998, 2009. ISBN 978-0-0521-83294-6.

10. *Slides from ECE135B Lectures, Winter 2011.* **Yu, Paul.** San Diego : UCSD, 2011.

7 Appendix A – Simulation Code

Simulation code for this assignment was written in Scilab, a mathematics-oriented programming language very similar to Matlab. The Scilab program is freely available and can be downloaded from http://www.scilab.org, hence it was chosen for this project.

7.1 Code for Calculating I_D vs V_{DS}

The below code was used to plot the value of I_D for different values of V_{DS}. V_T, W, and V_{GS} are given as fixed parameters.

```
function result = sim_mosfet(Vg, W, Vds, Vt)
	//This function computes the Id for a range of Vd (Vds) for a given MOSFET, with
potential
	//Vg applied to the gate. We use the gradual channel approximation in this calculator.

	//Physical Constants
	esi = 11.7 * 8.85D-14;
	eox = 3.9 * 8.85D-14;
	Nc_0 = 2.8D19;
	Nv_0 = 1.83D19;
	ni = 1.0D10;
	kT_0 = 0.0259;
	k = 8.617D-5 * 1.6D-19;
	Eg = 1.12;
	q = 1.6D-19;
	mu_n0 = 32500; //mobility in high-field model
	mu_nmax = 1400; //maximum, no-applied-field mobility
	vsat = 1D7; //saturation velocity for carriers, electrons in this case

	//Transistor parameters
	Na = 1.16D19;
	tox = 1.6D-9 * 1D2;
	Qt = 0 * q;
	T = 300;
	L_0 = 32D-7;
	strain_udel = 1.0; //Multiplicative factor for ueff, based on strained Si

	//Derived parameters
	Cox = eox / tox;
	phi_b = kT_0*log(Na/ni);
	m = 1+sqrt(esi * q * Na / (4*phi_b))/Cox;

	//Init result
	result = zeros(1, size(Vds,2));

	for i = 1:size(Vds,2);
		Vd = Vds(i);

		//Calculate effective field, and adjust mobility
		E_eff = sqrt( (Vd / L_0)**2 + (Vg / L_0)**2 );
		mu_n = min(mu_n0 * E_eff**(-1/3), mu_nmax);
		//printf("E_eff=%e, mu_n=%e\n", E_eff, mu_n);

		//Calculate saturation Vds
		Vdsat = ((Vg-Vt)/m)/(1+mu_n*(Vg-Vt)/(2*m*vsat*L_0));

		//Adjust channel length for channel length decrease
		//Lect 13 slide 5
		Fs = vsat / mu_n;
		L = L_0 - (esi/(q*Na))*(sqrt(Fs**2 + 2*(q*Na/esi)*(Vd - Vdsat)) - Fs);

		if(Vg <= Vt) then
			//Calculate current based on Sub-threshold conduction (3.40, p. 165)
```

```
                        result(i) = mu_n * Cox * (W/L) * (m-1) * (kT_0 ** 2) * %e**((Vg-
Vt)/(m*kT_0)) * (1-%e**(-Vd/kT_0));
                //elseif ((Vd / L) < (2*vsat / mu_n)) then //this doesn't work for some reason
                elseif (Vd < Vdsat) then
                        //Calculate current based on 3.77 from Taur/Ning (p. 188)
                        result(i) = (mu_n * Cox * (W/L) * ((Vg-Vt)*Vd -
(m/2)*(Vd**2)))/(1+((mu_n*Vd)/(2*vsat*L)));
                else
                        //Calculate current based on (3.94) & (3.95) (p. 191)
                        result(i) = (mu_n * Cox * (W/L) * (Vg-Vt)**2 / (2*m)) / (1 + mu_n*(Vg-
Vt)/(2*m*vsat*L));
                end
        end

endfunction
```

7.2 Code for Calculating I_D vs V_{GS}

The below code was used to plot the value of I_D for different values of V_{GS}. V_T, W, and V_{DD} are given as fixed parameters.

```
function result = sim_mosfet_vg(Vgs, W, Vd, Vt)
        //This function computes the Id for a range of Vg (Vgs) for a given MOSFET, with
potential
        //Vd applied to the drain. We use the gradual channel approximation in this calculator.

        //Physical Constants
        esi = 11.7 * 8.85D-14;
        eox = 3.9 * 8.85D-14;
        Nc_0 = 2.8D19;
        Nv_0 = 1.83D19;
        ni = 1.0D10;
        kT_0 = 0.0259;
        k = 8.617D-5 * 1.6D-19;
        Eg = 1.12;
        q = 1.6D-19;
        mu_n0 = 32500; //mobility in high-field model
        mu_nmax = 1400; //maximum, no-applied-field mobility
        vsat = 1D7; //saturation velocity for carriers, electrons in this case

        //Transistor parameters
        Na = 1.16D19;
        tox = 1.6D-9 * 1D2;
        Qt = 0 * q;
        T = 300;
        L_0 = 32D-7;
        strain_udel = 1.0; //Multiplicative factor for ueff, based on strained Si

        //Derived parameters
        Cox = eox / tox;
        phi_b = kT_0*log(Na/ni);
        m = 1+sqrt(esi * q * Na / (4*phi_b))/Cox;

        //Init result
        result = zeros(1, size(Vgs,2));

        for i = 1:size(Vgs,2);
                Vg = Vgs(i);

                //Calculate effective field, and adjust mobility
                E_eff = sqrt( (Vd / L_0)**2 + (Vg / L_0)**2 );
                mu_n = min(mu_n0 * E_eff**(-1/3), mu_nmax);
                //printf("E_eff=%e, mu_n=%e\n", E_eff, mu_n);

                //Calculate saturation Vds
                Vdsat = ((Vg-Vt)/m)/(1+mu_n*(Vg-Vt)/(2*m*vsat*L_0));
                Vdsat_subt = (Vg-Vt)/m + (L_0 * vsat)/mu_n - sqrt( ((Vg - Vt)/m)**2 + (L_0 * vsat
/ mu_n)**2 );
```

```
                //Adjust channel length for channel length decrease
                //Lect 13 slide 5
                Fs = vsat / mu_n;
                L = L_0 - (esi/(q*Na))*(sqrt(Fs**2 + 2*(q*Na/esi)*(Vd - max(Vdsat,0))) - Fs);

                //printf("Vg = %f, L = %e, mu_n = %e, Vdsat = %e\n", Vg, L, mu_n, Vdsat);

                if(Vg <= Vt) then
                        //Use n=inf approximation to make subthreshold current continuous
                        Vdsat = Vdsat_subt;
                        L = L_0 - (esi/(q*Na))*(sqrt(Fs**2 + 2*(q*Na/esi)*(Vd - max(Vdsat,0))) -
Fs);

                        //Calculate current based on Sub-threshold conduction (3.40, p. 165)
                        result(i) = abs( mu_n * Cox * (W/L) * (m-1) * (kT_0 ** 2) * %e**((Vg-
Vt)/(m*kT_0)) * (1-%e**(-Vd/kT_0)) );
                //elseif ((Vd / L) < (2*vsat / mu_n)) then //this doesn't work for some reason
                elseif (Vd < Vdsat) then
                        //Calculate current based on 3.77 from Taur/Ning (p. 188)
                        result(i) = (mu_n * Cox * (W/L) * ((Vg-Vt)*Vd -
(m/2)*(Vd**2)))/(1+((mu_n*Vd)/(2*vsat*L)));
                else
                        //Calculate current based on (3.94) & (3.95) (p. 191)
                        result(i) = (mu_n * Cox * (W/L) * (Vg-Vt)**2 / (2*m)) / (1 + mu_n*(Vg-
Vt)/(2*m*vsat*L));
                end
        end

endfunction
```

7.3 Code for Calculating I_D as Function of V_{GS} and V_T

The below code was used to compute I_{DS} as a function of both V_{GS} and V_T. V_{DD} and W are given as fixed parameters.

```
function result = sim_mosfet_3d(Vgs, W, Vd, Vts)
        //This function computes the Id for a range of Vg and Vt values; we can
        //generate a 3d plot in this manner

        //Physical Constants
        esi = 11.7 * 8.85D-14;
        eox = 3.9 * 8.85D-14;
        Nc_0 = 2.8D19;
        Nv_0 = 1.83D19;
        ni = 1.0D10;
        kT_0 = 0.0259;
        k = 8.617D-5 * 1.6D-19;
        Eg = 1.12;
        q = 1.6D-19;
        mu_n0 = 32500; //mobility in high-field model
        mu_nmax = 1400; //maximum, no-applied-field mobility
        vsat = 1D7; //saturation velocity for carriers, electrons in this case

        //Transistor parameters
        Na = 1.16D19;
        tox = 1.6D-9 * 1D2;
        Qt = 0 * q;
        T = 300;
        L_0 = 32D-7;
        strain_udel = 1.6; //Multiplicative factor for ueff, based on strained Si

        //Derived parameters
        Cox = eox / tox;
        phi_b = kT_0*log(Na/ni);
        m = 1+sqrt(esi * q * Na / (4*phi_b))/Cox;

        //Init result
        result = zeros(size(Vgs,2), size(Vts,2));
```

```
        //Outer loop - iterate over Vg values
        for i = 1:size(Vgs,2);
                Vg = Vgs(i);

                //Inner loop - iterate over Vt values
                for j = 1:size(Vts,2);

                        Vt = Vts(j);

                        //Calculate effective field, and adjust mobility
                        E_eff = sqrt( (Vd / L_0)**2 + (Vg / L_0)**2 );
                        mu_n = min(mu_n0 * E_eff**(-1/3), mu_nmax);
                        //printf("E_eff=%e, mu_n=%e\n", E_eff, mu_n);

                        //Calculate saturation Vds
                        Vdsat = ((Vg-Vt)/m)/(1+mu_n*(Vg-Vt)/(2*m*vsat*L_0));

                        //Adjust channel length for channel length decrease
                        //Lect 13 slide 5
                        Fs = vsat / mu_n;
                        L = L_0 - (esi/(q*Na))*(sqrt(Fs**2 + 2*(q*Na/esi)*(Vd - Vdsat)) - Fs);

                        //The (Vt+1mV) criteria was added to avoid a null when Vg == Vt due to the
                        //piecewise nature of our model
                        if(Vg < (Vt+0.001)) then
                                //Calculate current based on Sub-threshold conduction (3.40, p.
165)
                                result(i,j) = abs ( mu_n * Cox * (W/L) * (m-1) * (kT_0 ** 2) *
%e**((Vg-Vt)/(m*kT_0)) * (1-%e**(-Vd/kT_0)) );
                        //elseif ((Vd / L) < (2*vsat / mu_n)) then //this doesn't work for some
reason
                        elseif (Vd < Vdsat) then
                                //Calculate current based on 3.77 from Taur/Ning (p. 188)
                                result(i,j) = (mu_n * Cox * (W/L) * ((Vg-Vt)*Vd -
(m/2)*(Vd**2)))/(1+((mu_n*Vd)/(2*vsat*L)));
                        else
                                //Calculate current based on (3.94) & (3.95) (p. 191)
                                result(i,j) = (mu_n * Cox * (W/L) * (Vg-Vt)**2 / (2*m)) / (1 +
mu_n*(Vg-Vt)/(2*m*vsat*L));
                        end

                        if(result(i,j) < 1D-20)
                                printf("result = %e, Vg = %f, Vt = %f\n", result(i,j), Vg, Vt);
                        end

                end
        end

endfunction

function result = plot_fig7()
        //This function generates a SciLab plot for figure 7 of my ECE135B report

        Vgs = [0:0.05:1.4];
        Vts = [0.2:0.02:0.7];

        simres = sim_mosfet_3d(Vgs, 32D-7*2, 1.4, Vts);

        //Crease a "sheet" showing the cutoff voltage
        id_cutoff = zeros(size(Vgs,2), size(Vts,2)) + 49D-6;

        //Generate the plots
        f = scf();
        plot3d1(Vgs, Vts, simres);
        plot3d1(Vgs, Vts, id_cutoff);
        f.color_map = autumncolormap(32);
        f.anti_aliasing = "2x";

        //Set axes properties
        a = gda();
        //a.log_flags = "nnl";
```

```
        result = f;

endfunction
```

7.4 Code for Calculating W_{dm} as Function of N_A

The below code was used to create the W_{dm}vs N_A plot (Figure 6, section 4.3). It computes the depletion depth W_{dm} as a function of N_A.

```
function result = wdm_plot(Nas)
        //This function computes the Wdm of a MOSFET structure across a range of Na
        //values given by Nas

        //Physical Constants
        esi = 11.7 * 8.85D-14;
        Nc_0 = 2.8D19;
        Nv_0 = 1.83D19;
        ni = 1.0D10;
        kT_0 = 0.0259;
        k = 8.617D-5 * 1.6D-19;
        Eg = 1.12;
        q = 1.6D-19;

        //Transistor parameters
        T = 300;

        //Init result
        result = zeros(1, size(Nas,2));

        for i = 1:size(Nas,2);
                Na = Nas(i);

                result(i) = sqrt((4*esi*k*T*log(Na/ni))/(q**2 * Na));
        end

endfunction
```